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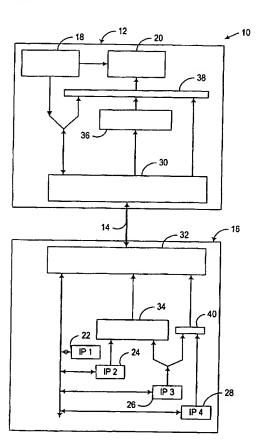
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(54) Title: DEDICATED ENCRYPTED VIRTUAL CHANNEL IN A MULTI-CHANNEL SERIAL COMMUNICATIONS INTERFACE



(57) Abstract: A data processing system, circuit arrangement, and method to communicate data over a multi-channel serial communications interface: such as a PCI-express connection (14) using a dedicated encrypted virtual channel from among multiple virtual channels supported by the communications interface (14). Encryption for the dedicated encrypted virtual channel is provided by a hardware encryption circuit (34) that is coupled to the interface, such that encryption may be performed at a relatively low level, and with substantial protection from compromise, particularly along chip boundaries. In one particular application, access control may be provided for a digital data stream using a multi-chip access control scheme that relies on one chip (148) to provide access control over a received digital data stream, with another chip (150) utilized to process the digital data stram once authorized to do so. A secure, multi-channel serial communications interface between the multiple chips re-encrypts a digital data stream that has been decrypted on the access control chip (148) using hardware encryption logic (162) disposed on the access control chip (148), communicates the re-encrypted digital data steam over a dedicated encryption virtual channel supported by the multi-channel serial communications interface, and decrypts the re-encrypted digital data steam using hardware decryption logic (164) disposed on the other chip (150).

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as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, Fl, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ,

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C. DOCUM	ENTS CONSIDERED TO BE RELEVANT			
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Ţ	MAYHEW D ET AL: "PCI express and advanced switching: evolutionary path to building next generation interconnects" PROCEEDINGS OF THE 11TH SYMPOSIUM ON HIGH-PERFORMANCE INTERCONNECTS-HOTI'03, 20 August 2003 (2003-08-20), pages 21-29, XP010657970 page 21, left-hand column - page 23, left-hand column page 25, left-hand column, paragraph 2.2.2		1-45	
<u> </u>	er documents are listed in the continuation of box C.	Patent family members are its	ted in annex.	
*A' document datining the general state of the art which is not considered to be of particular relevance *E' earlier document but published on or after the international filing date *L' document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) *O' document referring to an oral disclosure, use, exhibition or other means *P' document published prior to the international filing date but		 T later document published after the international filling date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken atone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. 		
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Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer Carnerero Álva	ro, F	

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